**Lab 5: Sequential Circuit Analysis**

**Primary Objectives**

1. Analyze multiple sequential circuits using timing diagrams

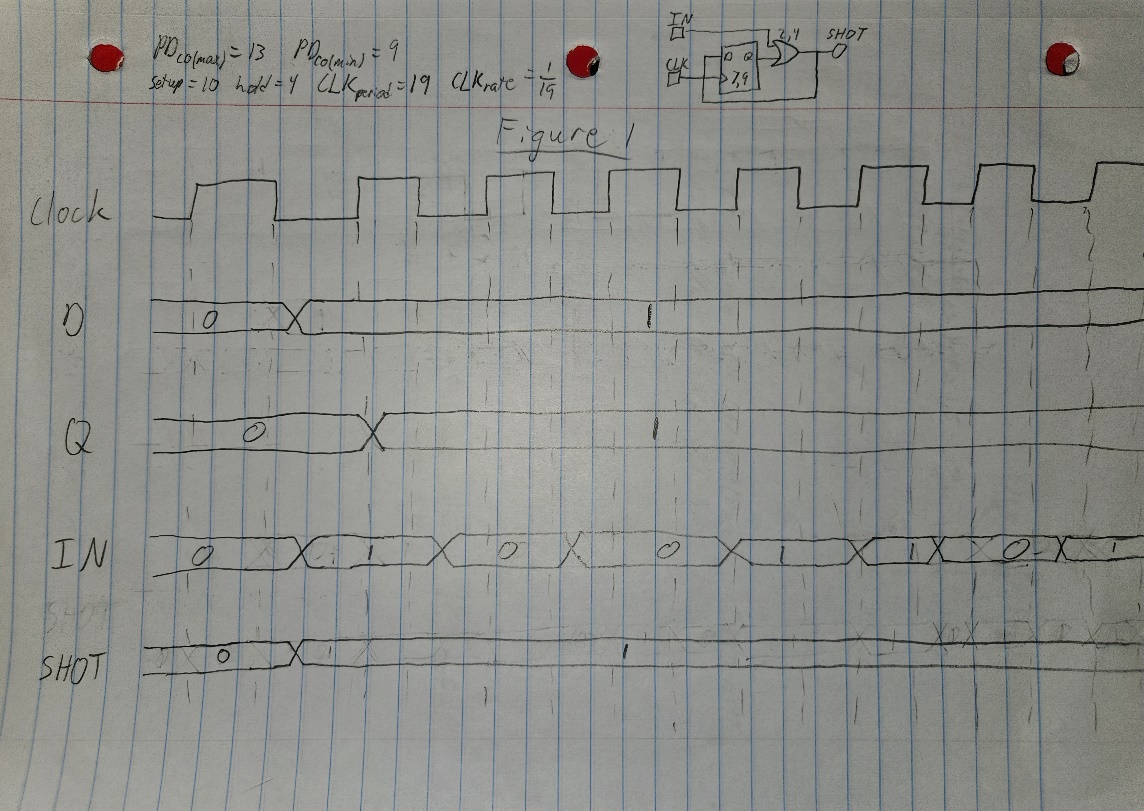
2. Analyze the function and states of the circuits

3. Implement the systems using the Logisim software

4. Calculate the timing data for the circuits

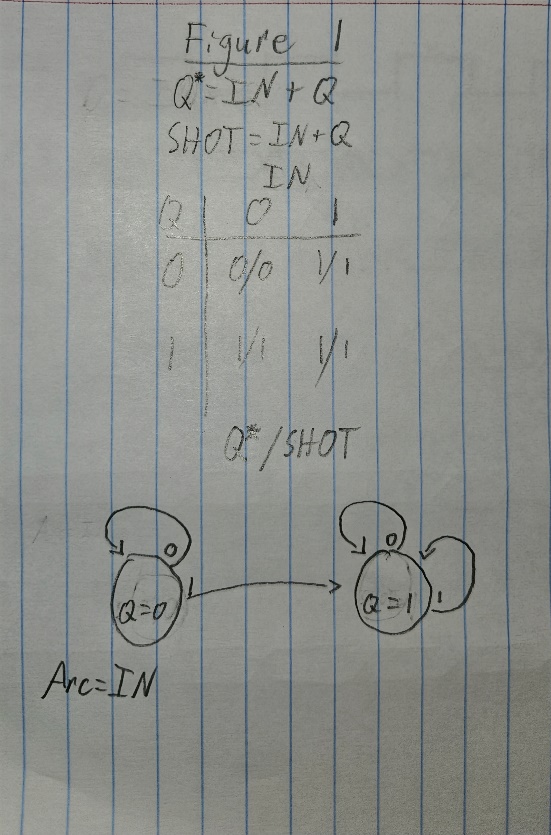
*Figure 1 Analysis*

Shown in Timing Analysis 1 is the hand-drawn timing diagram for Figure 1.



Timing Analysis 1

From this timing diagram, we can see that the output SHOT only changes on the positive clock edge if IN is 1. At this point, SHOT’s value becomes 1 and remains 1 regardless of what happens with the rest of the circuit. Shown below in States Analysis 1 is the change of the states of Q in Figure 1, dependent on IN and Q(t-1). The state diagram and table affirm the previous idea of Figure 1’s function.



States Analysis 1

Below are the Logisim implementation of Figure 1 and corresponding logging results. The logging results demonstrate the system’s function and confirm the previous idea that the circuit constantly returns a 1 as long as the clock has ticked while IN was turned on.

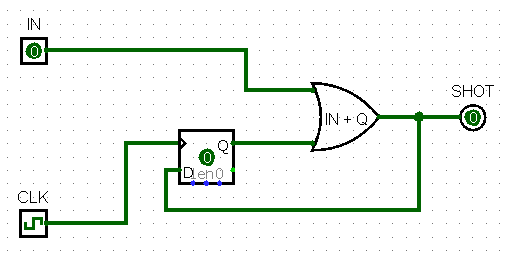


Figure 1 Implementation

A screenshot of a table

Description automatically generated

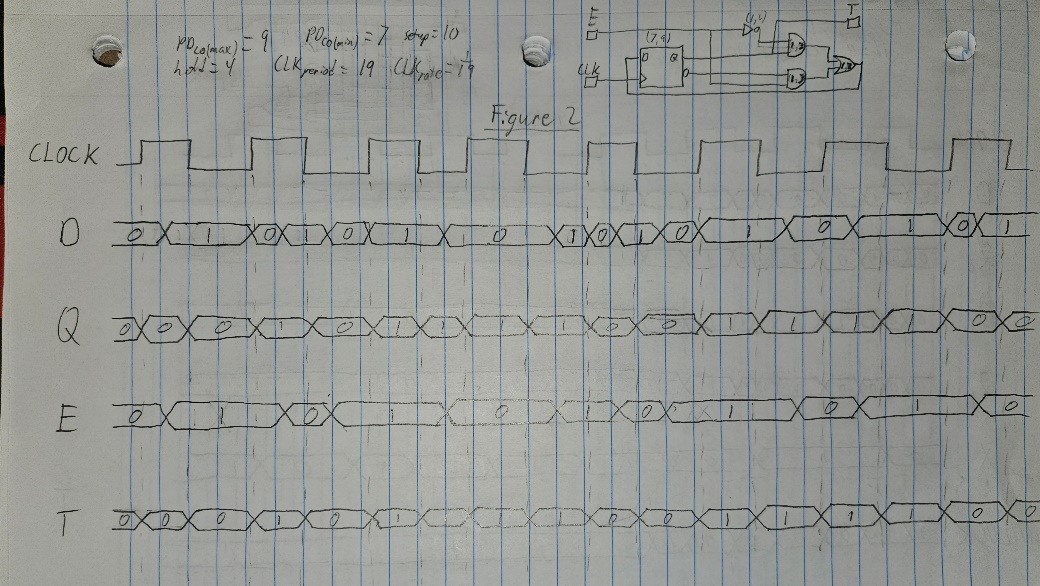
Log 1

Below is all the timing information for Figure 1 (in nanoseconds):

* Setup time, input to clock: 14
* Hold time, input to clock: 2
* Propagation delay, clock to output (min): 9
* Propagation delay, clock to output (max): 13
* Maximum clock rate of device: 1/23

*Figure 2 Analysis*

Shown in Timing Analysis 2 is the hand-drawn timing diagram for Figure 2.



Timing Analysis 2

From this timing diagram, we can see that the output T only changes on the positive clock edge if E is 1. At this point, T’s value alternates between 0 and 1 on every positive clock edge. If E is then turned off, T will hold whatever its previous value was, even when the clock ticks. Shown below in States Analysis 2 is the change of the states of Q in Figure 2, dependent on E and Q(t-1). The state diagram and table affirm the previous idea of Figure 2’s function.

A graphing of a mathematical equation

Description automatically generated with medium confidence

States Analysis 2

Below are the Logisim implementation of Figure 2 and corresponding logging results. The testing log demonstrates how E acts as a sort of enabler for the device, which just alternates T between 0 and 1 as long as it is turned on and outputs the previous value of T when it is not.

A diagram of a circuit

Description automatically generated

Figure 2 Implementation

A screenshot of a computer

Description automatically generated

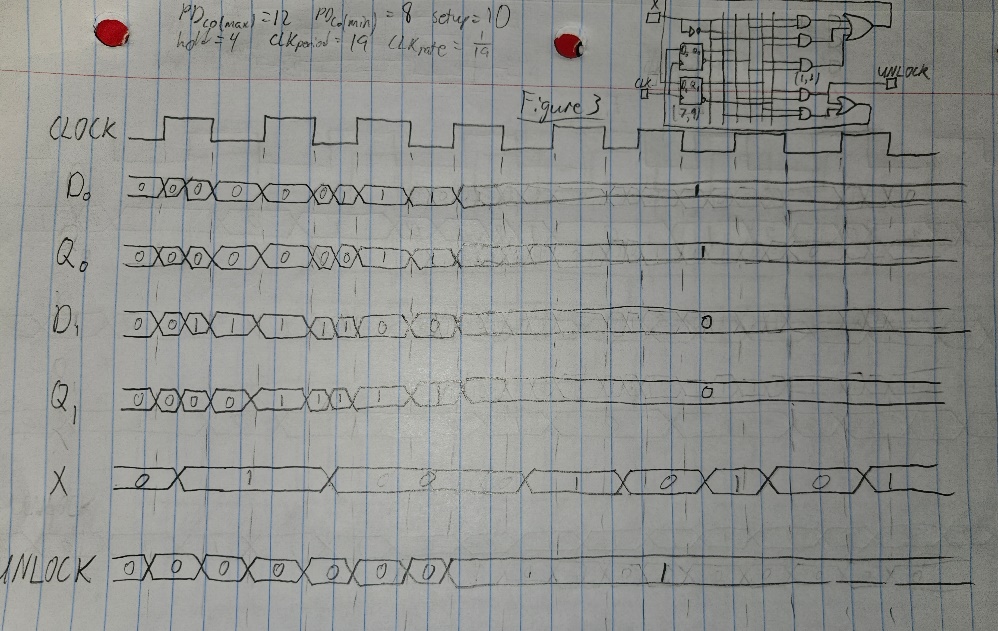
Log 2

Below is all the timing information for Figure 2 (in nanoseconds):

* Setup time, input to clock: 18
* Hold time, input to clock: 1
* Propagation delay, clock to output (min): 7
* Propagation delay, clock to output (max): 9
* Maximum clock rate of device: 1/27

*Figure 3 Analysis*

Shown in Timing Analysis 3 is the hand-drawn timing diagram for Figure 3.



Timing Analysis 3

From this timing diagram, we can see that the output UNLOCK only changes on the positive clock edge when Q0 is 1 and Q1 is 0. At this point, UNLOCK’s holds a 1 no matter what else happens in the device. Shown below in States Analysis 3 is the change of the states of Q0 and Q1 in Figure 3, dependent on E and Q0(t-1)/Q1(t-1). As can be seen in the diagram, when Q1 is 0 and Q0 is 1, the states will loop in 01, no matter the value of X.

A close-up of a graphing paper

Description automatically generated

States Analysis 3

Below are the Logisim implementation of Figure 3 and corresponding logging results. The testing log demonstrates how the device works in practice. UNLOCK can only become 1 if X has been 1 at some point in the past when the clock ticked. X must then be 0 for two consecutive clock ticks for UNLOCK to be 1.

A diagram of a circuit

Description automatically generated

Figure 3 Implementation

A screen shot of a number

Description automatically generated

Log 3

Below is all the timing information for Figure 3 (in nanoseconds):

* Setup time, input to clock: 19
* Hold time, input to clock: 2
* Propagation delay, clock to output (min): 8
* Propagation delay, clock to output (max): 12
* Maximum clock rate of device: 1/28